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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/619,051	07/18/2000	Robert S. Blackmore	POU920000126US1	9648

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EXAMINER	
CHOUDHARY, ANITA	
ART UNIT	**PAPER NUMBER**
2153	

DATE MAILED: 09/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/619,051	BLACKMORE ET AL.	
	Examiner	Art Unit	
	Anita Choudhary	2153	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 July 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The amendment filed on July 2, 2004 under 37 CFR 1.312 has been entered. New claims 3 and 4 are added.

Claims 1-4 are presented.

Response to Arguments

Applicant's arguments filed July 2, 2004 have been fully considered but they are not persuasive.

Applicant argues that Sethuram shows a "virtual register" which is opposite to the feature claiming, "real address information". The reasoning used to support this assertion incorporates the literal meaning of the word "virtual" to be considered the opposite of "real". While this may be true, upon further reading of the Sethuram patent, it is evident that virtual register taking in context with the Sethuram invention demonstrates a direct association to a real buffer address located at the host memory. For further support see column 4 lines 33-44, column 57-column 5 line 1, column 5 lines 10-20 and column 6 lines 34-46. Stated therein are steps used to transmit and receive messages according to a virtual circuit associated with a virtual register, wherein the virtual register maps the incoming data directly to buffers in the host memory. Several embodiments are shown for initializing virtual registers to map directly to buffers. For example, virtual register mappings are created at initialization (col. 4 lines 40-42), dynamically as data is received (col. 4 lines 42-44), or at the host processor itself Col. 6 lines 6-8). In considering these features, the virtual register acts similarly to an address table by mapping incoming virtual circuits to real addresses of user buffers located on host memory.

Although "virtual" may literally mean the opposite of "real", given the above findings, it is reasonable to consider that the virtual register actual indicates real address information of buffers located in the host memory. The direct memory access (DMA) further facilitates the transfer of data from the adapter memory to the host memory in accordance to the real buffer address information indicated by the virtual register.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Sethuram et al. (US 5,828,903).

Sethuram shows as system for transferring data between a network and host coupled to the network using a host adapter. The adapter is situated between the network and host system, wherein the adapter has a DMA engine and local memory. Sethuram shows:

transmitting incoming message from first data processing system (100-103) to a temporary memory (fig. 2b, 204) in an adapter, which is connected to said second data processing (host device) system (col. 4 lines 1-11).

transferring, from said adapter to said second data processing system, an indication that said temporary memory in said adapter contains the message received from said first data processing system (col. 9 lines 21-23).

transferring, from said second data processing system to said adapter, real address information (virtual register mapping to the host buffer) indicating desired target memory locations (host buffer) for said message (col. 4 lines 33-44, col. 4 line 57- col. 5 line 1, Note that each virtual register (VR1-VR8) maps to a free buffer (B1-B8), see col. 5 lines 15-20, fig. 3a and 3b).

transferring said message, from said temporary memory in said adapter, directly into said target memory locations in the memory of said second data processing system, said transfer occurring via direct memory access (col. 6 line 22-30 and 44-46).

transferring, from said adapter to said second data processing system, an indication that said target locations now contain the message received from said first data processing system (col. 6 line 54-56).

transmitting an acknowledgement of receipt of said message from said second data processing system to said first data processing system (col. 6 lines 47-50, col. 13 lines 53-55).

In referring to claim 2, Sethuram further discloses the step of advancing indicators in said first data processing system in preparation of transmitting another message, whereby a number of messages may be sent in rapid sequence (col. 9 lines 49-55).

In referring to claim 3, Sethuram shows:

establishing an association between said message and real address information indicating desired target memory locations for said memory (col. 5 lines 23-28 and col. 7 lines 26-41, Note that the virtual register can be associated with buffer on an "as needed" basis and the size of a packet data unit is determined in order to allocate the correct sized buffer);

transmitting incoming message from first data processing system (100-103) to a temporary memory (fig. 2b, 204) in an adapter, which is connected to said second data processing (host device) system (col. 4 lines 1-11).

transferring, from said adapter to said second data processing system, an indication that said temporary memory in said adapter contains the message received from said first data processing system (col. 9 lines 21-23).

transferring, from said second data processing system to said adapter, real address information (virtual register mapping to the host buffer, col. 4 lines 33-44, col. 4 line 57- col. 5 line 1, Note that each virtual register (VR1-VR8) maps to a free buffer (B1-B8), see col. 5 lines 15-20, fig. 3a and 3b).

transferring said message, from said temporary memory in said adapter, directly into said target memory locations in the memory of said second data processing system, said transfer occurring via direct memory access (col. 6 line 22-30 and 44-46).

transferring, from said adapter to said second data processing system, an indication that said target locations now contain the message received from said first data processing system (col. 6 line 54-56).

transmitting an acknowledgement of receipt of said message from said second data processing system to said first data processing system (col. 6 lines 47-50, col. 13 lines 53-55).

In referring to claim 4, Sethuram shows:

establishing an association between memory buffer areas in said data processing systems wherein said association includes specification of real address information at said second data processing system (col. 5 lines 23-28 and col. 7 lines 26-41, Note that the virtual register can be

associated with buffer on an "as needed" basis and the size of a packet data unit is determined in order to allocate the correct sized buffer);

transferring said message from said first data processing system to an adapter attached to said second data processing system together with a tag (virtual circuit #) which includes said association (col. 7 lines 51-62, col. 8 lines 20-28, col. 8 lines 52-56, Note that a virtual circuit number is associated or linked with a virtual register number which maps to real buffer address on host memory); and

transferring said message from said adapter which uses said tag (virtual circuit #) to transfer said message directly to memory locations (host buffer) in said second data processing system specified by said real address information (col. 4 lines 33-44, col. 4 line 57- col. 5 line 1, Note that each virtual circuit is associated a virtual register (VR1-VR8) which maps directly to a free host buffer (B1-B8), see col. 5 lines 15-20, fig. 3a and 3b).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anita Choudhary whose telephone number is (703) 305-5268. The examiner can normally be reached on 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glenton Burgess can be reached on (703) 305-4792. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Anita Choudhary
September 15, 2004

FRANTZ B. JEAN
PRIMARY EXAMINER